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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,505	08/01/2001	Toru Aoki	2001-0565A	5693

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	7

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/831,505	AOKI, TORU	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-4 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 10 May 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

Figures 4 and 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on May 10, 2001 has been considered by the examiner.

Specification

The disclosure is objected to because of the following informalities: The brief description of the drawings describes figure 6 as conventional (also on page 3 lines 3-5 of the background art designates figures 4 and 6 as conventional). This is not consistent, as these figures are not labeled as prior art.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chuang U.S. Patent No. 6,003,151 in view of Sawada et al. U. S. Patent No. 6,600,779.

As per claim 1, Chuang substantially teaches the claimed signal processor system in which a data string is retrieved from the optical storage disk and converted to a form compatible with storage in a digital memory. The retrieved data string is stored within a buffer memory while the retrieved data string is provided to an error detection circuit. Error detection is performed on the retrieved data string to determine if errors exist within the retrieved data string, with at least a portion of the error detection

operation performed while the retrieved data string is being stored into the buffer memory. The retrieved data string is transferred to the host computer system if the error detection operation determines that no errors are present in the retrieved data string. On the other hand, if the error detection operation determines that errors are present in the retrieved data string, then an error correction operation is performed on the retrieved data string prior to transferring the retrieved data string to the host computer. A variety of operations must be performed on the data read from the CD-ROM disk before the data can be provided to the data buses of the host computer system. These operations are generally familiar to those of ordinary skill in the art and include descrambling, reorganization, buffer storage, error correction, and error detection (column 1 lines 61-66 column 3 line 47 through column 4 line 19). Not explicitly disclosed is the controller for error free data.

However, in an analogous art, Sawada et al. teach a signal processor including several methods for use of controller in the error correction process in which a control circuit is provided that controls an error correcting performance of an error correcting apparatus receiving uncorrected data read from a first memory device, correcting the uncorrected data, and storing the data corrected in one of the first memory device and a second memory device. Data read and corrected is then provided to the host (column 7 line 14 through column 8 line18 column 11 line13-18). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the signal processor controller of Sawada et al. with the signal processor of Chuang. This would have been obvious as suggested by Sawada et al. because this

error correction process and control of such influences the speed at which this data is read and processed (column 4 lines 20-57).

As per claim 2, Sawada et al. teach an optical disk controller which reads one sector of data from the buffer memory and performs error correction interleave by interleave. Error correction includes (1) a step of generating a syndrome from one sector of data using the error correction code ECC, (2) a step of generating error position/value polynomials in accordance with the Euclidean algorithm using the syndrome, (3) a step of acquiring a solution for the error position/value polynomials by performing chien search, (4) a step of computing error positions and error values based on the solutions, and (5) a step of correcting errors based on the error positions and error values (column 42 lines 33-44 figure 68).

As per claims 3 and 4, Sawada et al. teach that when there is an uncorrectable interleave with many errors, the optical disk controller stops error correction on that interleave and corrects an error in the next interleave. When error correction at the positions 0 to 15 in the interleaves 1 to n is completed, it is determined if there is at least one error-uncorrectable interleave. When there is an error-uncorrectable interleave, error correction at the positions 0 to 119 in the interleaves (i+1) to n is carried out using the error correction code (ECC field) at the positions 0 to 119 in the interleaves (i+1) to n. That is, error correction is sequentially implemented on values at the positions 0 to 119 in the interleaves 1 to n. An error in each uncorrectable interleave is corrected in

this way. When there is no uncorrectable interleave, error correction is terminated immediately, and error correction on the next, new sector data will be implemented. If there is still an error-uncorrectable interleave, the same error correction is performed again. If there is an error-uncorrectable interleave even after error correction is performed a plurality of times (e.g., three times), error correction on that sector is terminated and the data in the buffer memory is marked as having errors. Thereafter, error values in the sector data stored in the buffer memory are rewritten with correct values in accordance with the error positions of each interleave. In response to a command from the microprocessor, the optical disk controller supplies the corrected data, temporarily stored in the buffer memory, to the computer via the external interface circuit (column 42 line 45 through column 43 line 5).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"Trellis-Based Postprocessing of Viterbi Decisions for Noise Decorrelation and Compensation of Nonlinear Distortion (with application to magnetic recording channels)" Agazzi, et al. 1996 IEEE International Conference on Communications, Volume: 1, 23-27 June 1996 Page(s): 566 -572 vol.1

This paper presents a concatenated decoding algorithm for partial response channels in which the inner decoder is a low-complexity suboptimal Viterbi decoder that operates in the presence of linear or nonlinear intersymbol interference and/or correlated noise, and the outer decoder is used to introduce non-redundant error correction (error correction in the absence of channel coding), by taking advantage of the knowledge of the components of the channel response neglected by the inner decoder. The postprocessor operates by searching a trellis where the number of states is determined by the maximum length of error events expected, and is independent of the length of the channel impulse response. This algorithm allows long channel responses, typically arising from noise decorrelation, to be efficiently decoded. The primary example used is the partial response class IV (PR IV) magnetic recording channel. When the postprocessor is used to compensate the nonlinearity of this channel, it typically yields a 2 dB gain over the (linear) PR IV Viterbi decoder. If, in addition, it is used for noise decorrelation, it yields a 3 dB gain.

U.S. Patent No. 6,266,712 Henrichs

This patent teaches an (ECC) "Error Correction Control" built into its "Optical Microhead And Disk Controller With SCSI Interface" (FIGS. 5, 63A, 63B, and 63C). The Error Correction Codes executed during host-requested read-data or write-data disk-operations are used by both Disk Controllers (FIGS. 4 and 5), and are based upon a Reed-Solomon encoder/decoder circuit's calculated error results.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Cynthia Britt
Examiner
Art Unit 2133

CHB

ALBERT DECADY
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